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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,214	04/01/2004	Daniel Bensahel	S1022.81113US00	7308

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EXAMINER
RAO, G NAGESH

ART UNIT	PAPER NUMBER
1722	

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08/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/816,214	BENSAHEL ET AL.	
	Examiner	Art Unit	
	G. Nagesh Rao	1722	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1 .1 14

1) A request for continued examination under 37 CFR 1 .1 14, including the fee set forth in 37 CFR 1 .17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1 .1 14, and the fee set forth in 37 CFR 1 .17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114.

Applicant's submission filed on 7/10/07 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2) Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kazuki (JP 2002-359189) in view of Tuppen (US Patent No. 5,279,687).

Examiner is noting that an English translation from JPO Database has been previously provided on 9/6/06 office action for applicant's consideration and review.

Kazuki 189 teaches the process for fabrication of a heteroatomic layer semiconductor structure. Whereby the substrate which is Si and will read upon the term wafer is indented with V-Like groove structures in the surface that reads on applicant's ring of discontinuities (since applicant's pointedly remark the basis of this term is in the specification whereby on page 4 of the applicant's specification in the "Detailed Description" the ring of discontinuity is defined as "surface or groove irregularity") thereby in its broadest sense read upon by the "indentations" of Kazuki 189 which would also constitute as being a "rough area", where thereafter formation of indentations as defined, a SiGe layer is deposited on said substrate whereby forming via the epitaxial process a heteroatomic crystal structure due to the inherently defined method of layering a different material (SiGe) over the Si substrate (i.e. wafer). Furthermore the multiple groove structures formed in the Si substrate (forming in plurality form an inherent ring of discontinuity) denote it reading on a "Si trench" and the groove indentation structures actively formulate a particle area intended to contain at least one elementary component, whereby an additional crystal semiconductor layer of Si is

deposited ontop of the SiGe heteroatomic layer (As noted in Fig. 2). Furthermore Kazuki 189 teaches the slot arrangement via the indentations take on a "grid structure" to allow for "square device field" to be formed in order to advantageously optimize the cutting of the wafer into the chip devices, which are and have always been known to be square in this field of microelectronic fabrication (See Figure 3). Finally Kazuki 189 iterates that the distance parameters for the groove-like indentations in the substrate are going to range in .3-3 micrometer range and 200 micrometer of less range, given the mean square deviation as applicant's claim is in the range of 10-30 nm, Kazuki 189 when applying the variating values can provide for numerical calculations that may fall within the 10-30 nm range, in particular since the teachings denote the 200 micrometer limitation or less. Furthermore this can obviously be deviated based on routine experimentation for smaller levels of workspace given the sophisticated advancement of micro and nanotechnology in the semiconductor fabrication process (See Sections 0001-0056 and Figs. 1-8).

However because Kazuki 189 does not outright state in the teachings that the Si wafer and SiGe layer as being "single-crystal" rather referring to the materials as crystalline in nature, but it is inherently presumed that the structures worked upon would be of single crystal nature, given the fact that the Si wafer is formed

via CZ (Czochralski technique) well known for single crystal structure growth processes.

In analogous art pertaining as well to the manufacturing of heteroatomic crystal solid state devices, Tuppen 687 does teach similar techniques as disclosed by Kazuki 189 but specifically stating the use of one or more single crystal materials onto a substrate utilizing MBE or MOVPE techniques. Furthermore Tuppen 687 also teaches a range of $10^6 - 10^{10}$ cm^{-2} giving an average distance of .1-10 microns. Therefore anticipating the mean square deviation value of 10-30 nm as claimed by applicant (See Figs 1-5, Abstract, and Cols 1-6 Lines 1-68).

It would therefore be obvious to one having ordinary skill in the art at the time of the present invention to more so realize based on the known teachings of Tuppen 687 combined with Kazuki 189 that in order to fabricate these already lattice mis-matched crystalline structures, that it is best if the device is fabricated with a homogenous lattice structure of build given the particular known fact that the epi-layers built on the substrate may differ immediately in material structure. Furthermore Tuppen 687 reiterates as well emphasizes on what is inherently understood by Kazuki 189.

Response to Arguments

3) Applicant's arguments filed 7/10/07 have been fully considered but they are not persuasive. Upon review of the arguments and discussions with applicant's representative and now in light of the amended claims, examiner has purported a new set of rejections.

With respect to the prior set of claims, there was no clear specified order as to what occurred when and given the claim utilized the word "comprising" rather than "consisting" provided for a more broad and open interpretation towards what steps occurred when in the claim. Applicants have noted that the specification is what entails the only limited breakdown, whereas examiner disagrees, because the specification as applicant noted is intended to provide guidance, but that is it, just "guidance". The only time it is appropriate for the specification to be taken into account for claim interpretation and read into claim language consideration is via "means or step plus function" language as set forth by USC 112 6th Paragraph.

Now that this stated and clarified, for all intensive purposes examiner reviewed once again applicant's specification and found a broad view on the term "ring of discontinuity" which examiner has cited as basis for interpretation in the prior art rejection. The term referring to surface irregularities in the substrate, and that can be attributed to a variety of reasons from scribing the surface to pattern

etching into the substrate to inherent surface dislocations that exist in crystalline materials, (Examiner comment, there is no such thing as a "perfect-defect free" material, there are means that strive towards it, but not until nano and atomistic technology can it be unrefutably denoted as "perfec-defect free" material).

The basis of the rejection stems down to applicant's claim that the substrate is marked by a ring of discontinuity formed prior to the epitaxy layering of single crystal semiconductor material, in other words a Si substrate with the likes of a roughness pattern or just a pattern that denotes it from being smooth and consistent and a SiGe layer built ontop of the Si Substrate. Thereafter trenches formulated in the epitaxy layer, essentially forming little pocket squares for soon to be "micro-chip" like devices and ontop of the SiGe layer is a Si layer. Of course all the layers have to be composed of single crystal layers.

Kazuki 189 essentially taught everything, but the translation did not mention "single crystal", it did mention crystalline materials but not single crystal. As well the use of epitaxial process which is conventionally defined as "the growth on a crystalline substrate of a crystalline substance that mimics the orientation of the substrate". Thereby denoting that it would make relative inherent sense to use single crystal for the entire structure, considering the wafer is material product resulting from a Cz methods, known for producing monocrystalline ingots.

In order to provide the best explanation and rejection out there, examiner relies on the Tuppen 687 to back up the Kazuki 189, given the relative same degree of teachings and absolutely same concepts of technology derivation. It is common sense to apply the two teachings together and it is obvious to one having ordinary skill in the art to find said claims obvious if not already basically anticipated by Kazuki 189's teachings.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to G. Nagesh Rao whose telephone number is (571) 272-2946. The examiner can normally be reached on 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yogendra Gupta can be reached on (571)272-1316. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700

GNR